IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) Method for measuring the delay time of at least one signal line ~~(10-i)~~ connecting a memory buffer ~~(1)~~ with a memory module ~~(1-i)~~ comprising the following steps:

(a) sending a measurement start command from said memory buffer ~~(1)~~ to said memory module ~~(2-i)~~ and simultaneously starting an integration circuit ~~(18-i)~~ provided within said memory buffer ~~(1)~~;

(b) transmitting a measurement pulse via said signal line ~~(10-i)~~; and

(c) stopping the integration circuit ~~(18-i)~~ when the measurement pulse transmitted via said signal line ~~(10-i)~~ is detected by a pulse detector ~~(13-i)~~ provided within said memory buffer ~~(1)~~, wherein the integrated value of the integration circuit ~~(18-i)~~ indicates the delay time ~~($DT_i$)~~ of said signal line ~~(10-i)~~.

2. (Currently Amended) The method according to claim 1, wherein a measurement pulse generator ~~(7)~~ provided within said memory module ~~(2-i)~~ is activated after reception of the measurement start command by said memory module ~~(2-i)~~ to transmit a measurement pulse via said signal line ~~(10-i)~~ to said memory buffer ~~(1)~~.

3. (Currently Amended) The method according to claim 1, wherein a measurement pulse generator ~~(7)~~ provided within said memory buffer ~~(1)~~ is activated simultaneously with the integration circuit ~~(18-i)~~ when the measurement start command is sent to said memory module ~~(2-i)~~ to transmit a measurement pulse via said signal line ~~(10-i)~~ to said memory module ~~(2-i)~~.

4. (Currently Amended) The method according to claim 3, wherein the memory module ~~(2-i)~~ retransmits the measurement pulse received via said signal line ~~(10-i)~~ back to the memory buffer ~~(1)~~ when the memory module ~~(2-i)~~ has received the measurement start command.

5. (Currently Amended) The method according to claim 1, wherein the measurement start command is sent from said memory buffer (1) to said memory modules (2-i) via a control line of a command and address bus.

6. (Currently Amended) The method according to claim 2 or 3, wherein the measurement pulse generator (7) is clocked by a clock signal (CLK) having a predetermined clock period ($T_{CLK}$).

7. (Currently Amended) The method according to claim 6, wherein the integration circuit (18-i) is supplied with a phase adjusted clock signal (CLK') to integrate time fractions ($T_{CLK}/m$) of the clock period ($T_{CLK}$) of said clock signal (CLK) to the delay time ($DT_i$) of said signal line (10-i).

8. (Currently Amended) The method according to claim 7, wherein the clock signal (CLK) is generated by a clock signal generator (16).

9. (Currently Amended) The method according to claim 1, wherein the measured delay time of said signal line (10-i) is stored in a signal line delay memory (22) provided within said memory buffer (1).

10. (Currently Amended) The method according to claim 9, wherein a delay time compensation unit (12) provided within said memory buffer (1) is adjusted depending on the delay time ($DT_i$) which is stored in said signal line memory (22) such that all signal lines (10-i) connecting said memory buffer (1) to different memory modules (2-i) comprise an equal standard time delay ($DT_{set}$).

11. (Original) The method according to claim 1, wherein the signal line is a data line of a bi-directional data bus.

12. (Currently Amended) The method according to claim 1, wherein the measurement start command is generated by a control logic (3) of said memory buffer (1).

13. (Currently Amended) A memory buffer for a memory module board which is connected via a signal line ~~(10-i)~~ to a plurality of memory modules ~~(2-i)~~ mounted on said memory module board having different signal line lengths, wherein the memory buffer ~~(1)~~ comprises for each signal line ~~(10-i)~~ a corresponding integration circuit ~~(18-i)~~ for integrating the transmission time of a measurement pulse transmitted via said signal line ~~(10-i)~~ between said memory buffer ~~(1)~~ and a memory module ~~(2-i)~~ connected to said signal line ~~(10-i)~~.

14. (Currently Amended) The memory buffer according to claim 13, wherein the memory buffer ~~(1)~~ comprises a control logic ~~(3)~~ which sends a measurement start command to the memory modules ~~(2-i)~~ via a control line ~~(4)~~ of a command and address bus ~~(CA)~~.

15. (Currently Amended) The memory buffer according to claim 13, wherein the signal line ~~(10-i)~~ is a data line of a bi-directional data bus.

16. (Currently Amended) The memory buffer according to claim 13, wherein each integration circuit ~~(18-i)~~ is connected to the control logic ~~(3)~~ to receive a start signal when the measurement start command is sent to the memory modules ~~(2-i)~~.

17. (Currently Amended) The memory buffer according to claim 13, wherein the memory buffer ~~(1)~~ comprises a measurement pulse detector ~~(13)~~ which detects a measurement pulse received via said signal line ~~(10-i)~~.

18. (Currently Amended) The memory buffer according to claim 13, wherein the integration circuit ~~(18-i)~~ of a signal line ~~(10-i)~~ is connected to a corresponding measurement pulse detector ~~(13-i)~~ of said signal line ~~(10-i)~~ to receive a stop signal when a measurement pulse is detected by said pulse detector ~~(13-i)~~.

19. (Currently Amended) The memory buffer according to claim 13, wherein the memory buffer ~~(1)~~ comprises a signal line delay memory ~~(22)~~ for storing the integrated values of all integration circuits ~~(18-i)~~ provided within said memory buffer ~~(1)~~ as delay times ~~($DT_i$)~~ of the corresponding signal lines ~~(10-i)~~.

20. (Currently Amended) The memory buffer according to claim 13, wherein the memory buffer (1) comprises a delay compensation unit ~~(12)~~ which compensates the delay times ~~($DT_i$)~~ of the signal lines ~~(10-i)~~ depending on the delay times stored in said signal line delay memory ~~(22)~~ to provide an equal standard time delay for all signal lines ~~(10-i)~~ of said memory buffer ~~(1)~~.

21. (Currently Amended) The memory buffer according to claim 13, wherein the integration circuits ~~(18-i)~~ are supplied with a phase adjusted clock signal ~~(CLK')~~ generated by a clock phase generator ~~(27)~~ to integrate time fractions ~~($T_{CLK}/m$)~~ of a clock period ~~($T_{CLK}$)~~ of a clock signal ~~(CLK)~~ generated by a clock signal generator ~~(16)~~ provided within said memory buffer ~~(1)~~.

22. (Currently Amended) The memory buffer according to claim 13, wherein the memory buffer ~~(1)~~ comprises a measurement pulse generator ~~(7)~~ which transmits a measurement pulse via the signal line ~~(10-i)~~ when the control logic (3) sends a measurement start command to the memory modules ~~(2-i)~~.

23. (Currently Amended) The memory buffer according to claim 13, wherein the delay compensation unit ~~(12)~~ is connected via signal lines ~~(24)~~ to a microcontroller ~~(25)~~ mounted on a motherboard.

24. (Currently Amended) The memory buffer according to claim 13, wherein the memory modules ~~(2-i)~~ are DRAMs.